Real-World Pearls of Wisdom in High Performance Parallelism

Developers preparing for the next generation of Intel® Xeon Phi™ technology—codenamed “Knights Landing”—have all the more reason to learn new ways to exploit higher levels of parallelism from processors and coprocessors for optimization and high performance.

*High Performance Parallelism Pearls: Multicore and Many-core Approaches*, released last November, walks users through real-world examples—including source code—of how to leverage parallelism on processors and coprocessors using a standard set of programming methods.

Building off the momentum of their previous book, *Intel® Xeon Phi™ Coprocessor High-Performance Programming*, authors and Intel parallelism evangelists James Reinders and Jim Jeffers found an opportunity to create a “cookbook” of the inventive ways that numerous experts spanning a diversity of industries get the most from Intel® multicore and many-core processors.
Experts from around the globe

The roster of 69 contributors comprises a Who's Who of HPC experts from around the world representing academia (University of Tennessee, KU Lenven in Belgium, King Abdullah University of Science and Technology in Saudi Arabia); research institutions (Oak Ridge National Laboratory, Zuse Institute Berlin, CERN Norway, Danish Meteorological Institute); private consulting firms (QuickThread Programming, LLC, TechEnablement.com), and, of course, Intel Corporation.

As it covers a breadth and depth of subjects, those seeking parallel programming “pearls” of wisdom need not dig much. The 502-page book is separated into 28 chapters, with titles such as:

- Better Concurrency and SiDM on HBM
- Concurrent Kernal Offloading
- Heterogenous Computing with MPI
- Integrating Intel Xeon Phi Coprocessors into a Cluster Environment
- Portable Performance with OpenCL™

Each chapter shows in detail how to code for high performance. The source code sets from each example also are available for download on the book’s website, lotsofcores.com, which includes news and updates on the book from the authors.

With the industry striving for open standards to push for innovation, it’s no surprise that a second volume of High Performance Parallelism Pearls is in the works.

Buy High Performance Parallelism Pearls: Multicore and Many-core Programming Approaches now on Amazon.com or the Elsevier Store.

Optimization Notice

Intel’s compilers may or may not optimize to the same degree for non-Intel microprocessors for optimizations that are not unique to Intel® microprocessors. These optimizations include SSE2, SSE3, and SSSE3 instruction sets and other optimizations. Intel does not guarantee the availability, functionality, or effectiveness of any optimization on microprocessors not manufactured by Intel. Microprocessor-dependent optimizations in this product are intended for use with Intel microprocessors. Certain optimizations not specific to Intel® microarchitecture are reserved for Intel microprocessors. Please refer to the applicable product User and Reference Guides for more information regarding the specific instruction sets covered by this notice.

Notice revision #20110804