Additional Intel® Advanced Vector Extensions 512 (Intel® AVX-512)

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The Intel® Architecture Instruction Set Extensions Programming Reference includes the definition of additional Intel® Advanced Vector Extensions 512 (Intel® AVX-512) instructions.

As I discussed in my first blog about Intel AVX-512 last year, Intel AVX-512 will be first implemented in the future Intel® Xeon Phi™ processor and coprocessor known by the codename *Knights Landing*.

We had committed that Intel AVX-512 would also be supported by some future Intel® Xeon® processors scheduled to be introduced after Knights Landing. These additional documented instructions will now appear in such processors, along with most Intel AVX-512 instructions published previously.

The new instructions enrich the operations available as part of Intel AVX-512. These are provided in two groups. A group of byte and word (8- and 16-bit) operations known as Byte and Word Instructions, indicated by the AVX512BW CPUID flag, enhance integer operations. It is notable that these do make use of all 64 bits in the mask registers. A group of doubleword and quadword (32- and 64-bit) operations known as Doubleword and Quadword Instructions, indicated by the AVX512DQ CPUID flag, enhance integer and floating-point operations.

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An additional orthogonal capability known as Vector Length Extensions provide for most AVX-512 instructions to operate on 128 or 256 bits, instead of only 512. Vector Length Extensions can currently be applied to most Foundation Instructions and the Conflict Detection Instructions, as well as the new Byte, Word, Doubleword, and Quadword instructions. The AVX-512 Vector Length Extensions are indicated by the AVX512VL CPUID flag. The use of Vector Length Extensions extends most AVX-512 operations to also operate on XMM (128-bit, SSE) registers and YMM (256-bit, AVX) registers. The use of Vector Length Extensions allows the capabilities of EVEX encodings, including the use of mask registers and access to registers 16..31, to be applied to XMM and YMM registers, instead of only to ZMM registers.

Emulation for Testing, Prior to Product

In order to help with testing of support, the Intel® Software Development Emulator has been extended to include these new Intel AVX-512 instructions and is available at: http://www.intel.com/software/sde.

Intel AVX-512 Family of Instructions

Intel AVX-512 Foundation Instructions will be included in all implementations of Intel AVX-512. While the Intel AVX-512 Conflict Detection Instructions are documented as optional extensions, the value for compiler vectorization has proven strong enough that they will be included in Intel Xeon processors that support Intel AVX-512. This makes Foundation Instructions and Conflict Detection Instructions both part of all Intel AVX-512 support for both future Intel Xeon Phi coprocessors and processors and future Intel Xeon processors.

Knights Landing will support Intel AVX-512 Exponential and Reciprocal Instructions and Intel AVX-512 Prefetch Instructions, while the first Intel Xeon processors with Intel AVX-512 will support Intel AVX-512 Doubleword and Quadword Instructions, Intel AVX-512 Byte and Word Instructions, and Intel AVX-512 Vector Length Extensions. Future Intel Xeon Phi coprocessors and processors (after Knights Landing) may offer additional Intel AVX-512 instructions, but should maintain a level of support at least comparable to Knights Landing (Foundation Instructions, Conflict Detection Instructions, Exponential and Reciprocal Instructions, and Prefetch Instructions). Likewise, the level of Intel AVX-512 support in the Intel Xeon processor family should include at least Foundation Instructions, Conflict Detection Instructions, Byte and Word Instructions, Doubleword and Quadword Instructions, and Vector Length Extensions whenever Intel AVX-512 instructions are supported. Assuming these baselines in each family simplifies compiler designs and should be done.

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Intel AVX-512 Support

Release of detailed information on these additional Intel AVX-512 instructions helps enable support for tools, applications, and operating systems by the time products appear. We are working with open source projects, application providers, and tool vendors to help incorporate support. The Intel® compilers, libraries, and analysis tools have strong support for Intel AVX-512 today. Updates, planned for November 2014, will provide support for these additional instructions as well.

Intel AVX-512 Documentation

The Intel AVX-512 instructions are documented in the Intel® Architecture Instruction Set Extensions Programming Reference. Intel AVX-512 is detailed in Chapters 2–7.

For more complete information about compiler optimizations, see our Optimization Notice.

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